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Abstract

- Design and testing of RFIC. Tested RF Modules in Lab. RF System Design. Design of Digital Integrated Circuit with multiple generations of CMOS technologies in different harsh environment.

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RF and Electrical Engineer.

Please note:

There is no company confidential or otherwise any propriety information on any of these slides.

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Summary:

- Experience in SSPA, RF System Design and Test.
- Lab Experience Testing RF-Modules with VNA, SG, SA. Support troubleshooting with the manufacturing.
- Experience with RFIC as well as High Speed Digital Design; Simulation, Development and Analysis.
- Experience with Full Product Cycle of Digital Design.
- Experience with IC Circuit and Layout, Verification using SPICE, DRC/LVS/NOISE using state of the art EDA tools from Cadence, Synopsys & Mentor G.

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Design Overview on SSPA

- Design Overview of Boeing Solid State Power Amplifier (SSPA) for Multiport Transceiver Systems for SLS.
- Design Overview of Solid State Power Amplifier (SSPA) and Multiport Transceiver Systems for Boeing Space. Proposed techniques to mitigate challenges to improve:
  - Linearity, Gain.
  - Power Consumption.
  - AM to PM Conversion in the SSPA.

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Design Overview on SSPA (Power)

- Power Design SSPA:
- 120 Watt and 240 Watt.
- 2 SSPAs One for … and another for …System
- 100+ Watt 8PSK:
- The RF output power capability of the SSPA. More compressed. And Different Filter at the Output.
- 200+ Watt: More Power, More Linear and A different type of Harmonic Filter.
- Helped Mitigate Power Consumption and Power Dissipations. Familiar with Pre-Distortion Technique.

SSPA (AM to PM Conversion)

- The goal is to minimize the AM to PM Conversion in SSPA so that any amplitude modulation on the Input signal does not result in phase modulation at the Output.
- The device capacitances and feedback mechanisms vary with input power, causing phase shifts as amplitude changes.
- AM to PM Conversion means what? AM to PM Conversion means the behavior of the SSPA.
- It was XY° / dB, big. Suggested techniques to make it zz° / dB (Lower).

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RF System design.

- MADL (Multifunction Advanced Data Link) M-RE ((Multifunction Advanced Data Link) – Remote Electronics)). For the US Govt Cust.
- RF System Design: Measured P1dB/IP3. Black-Box.
- Even though all the individual RF modules worked well, we solved the challenges and debugged in the System level.

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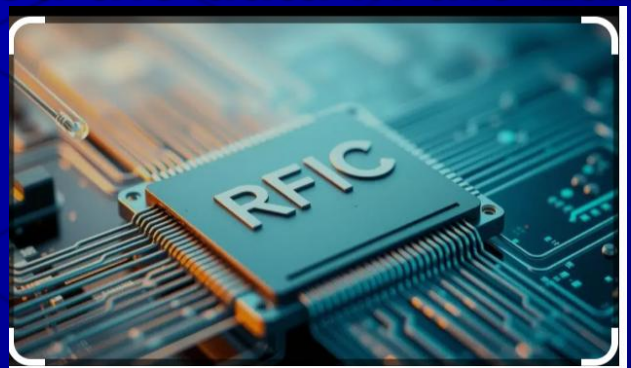
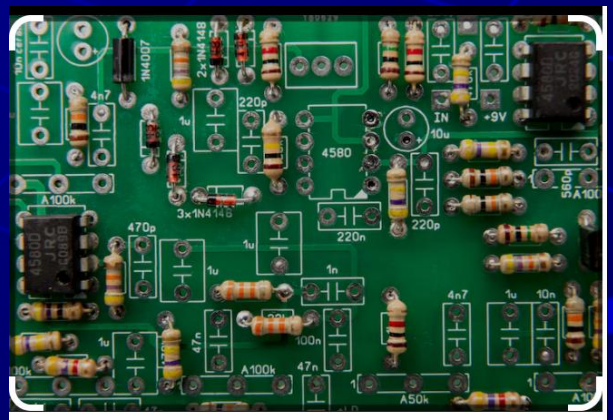
Lab Experience: Verified RF Modules for the requirements of customers.

- Tested RFIC Modules such as LNA, HPA, SYX, Up-Dwn Converters. Measured RR (S11), Gain (S21), P1dB, Linearity and Harmonics.

- Experienced with VNA, SG, SA and programmed Digital Boards with LabView Software.

- Written the Lab Procedures. Followed that Lab procedures. Then took the measurements and analyzed the data in the Lab.





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- Debugging efforts on the RF-Lab with better procedures, correct measurements verified the modules wrt their specs.
- RF System Design: Measured P1dB/IP3 for BBox. Programmed Digital boards with LabView Software.
- Mitigated challenges on the RF-Boards; while the components on it were individually working.
- Presented the Lab report to the management.

System on a Chip, MtM (More than Moore's law)

Completed the RF System Design: Link Budget Analysis on 3-D Heterogeneous packaging for Space.

Heterogeneous Packaging: RF Link Budget Analysis on Gain, Return Loss, (RR, S_{11}), Linearity and Harmonics.

In addition, tested the Gain (S_{21}) Return Loss, (RR, S_{11}), Nonlinearity Checks.

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Robust and Reliable Design

- Designed and tested both Digital and RF Modules with the Safety, Robustness and Longevity.
  - EM, IR drop and Noise
  - Grounding, Shielding, Filtering & Twisted-Pair.
  - Failure analysis in a harsh environment
- Familiarity with mitigating issues such as:
  - Electromagnetic Interference
  - EMC and EMI issues

RFIC Design/Testing for Space Application

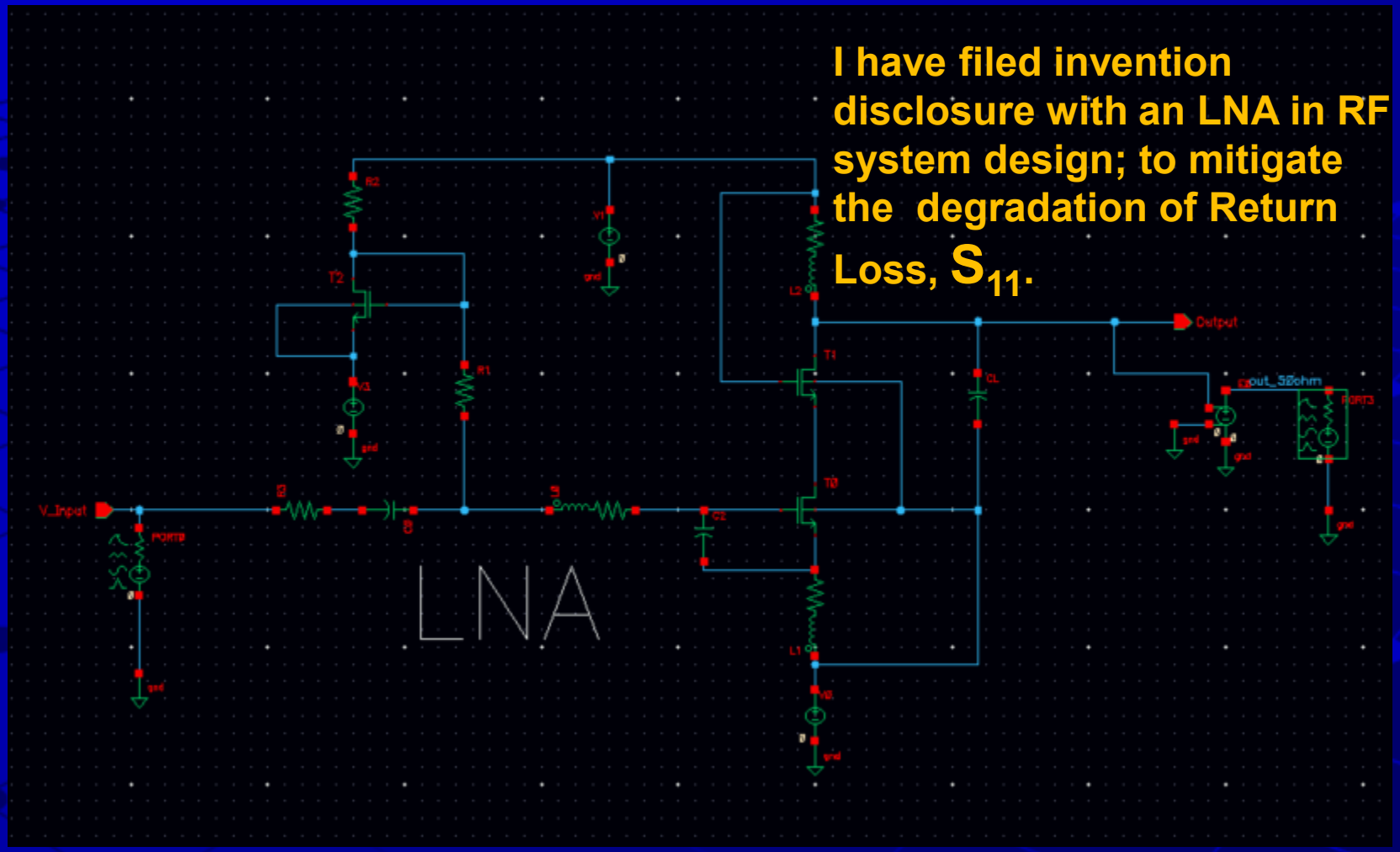
SITUATION/TASKS: Started the RFIC design and 3-D Heterogeneous packaging for Space application, after I had installed the PDK.

ACTIONS: I had to learn two tools' ADS (from Keysight) and RF-Spectra (from Cadence) rather quickly. Also used HFSS to analyze gain, linearity on the 3-D Heterogeneous (MtM) project.

RESULTS:

Successfully Completed the RFIC Project: Designed LNA, PA (next page).

Circuit of Low Noise Amplifier



FREQUENCY OF f the LNA @ 1 GHz

Gain: 23 dB

Noise Figure = 4.0 dB

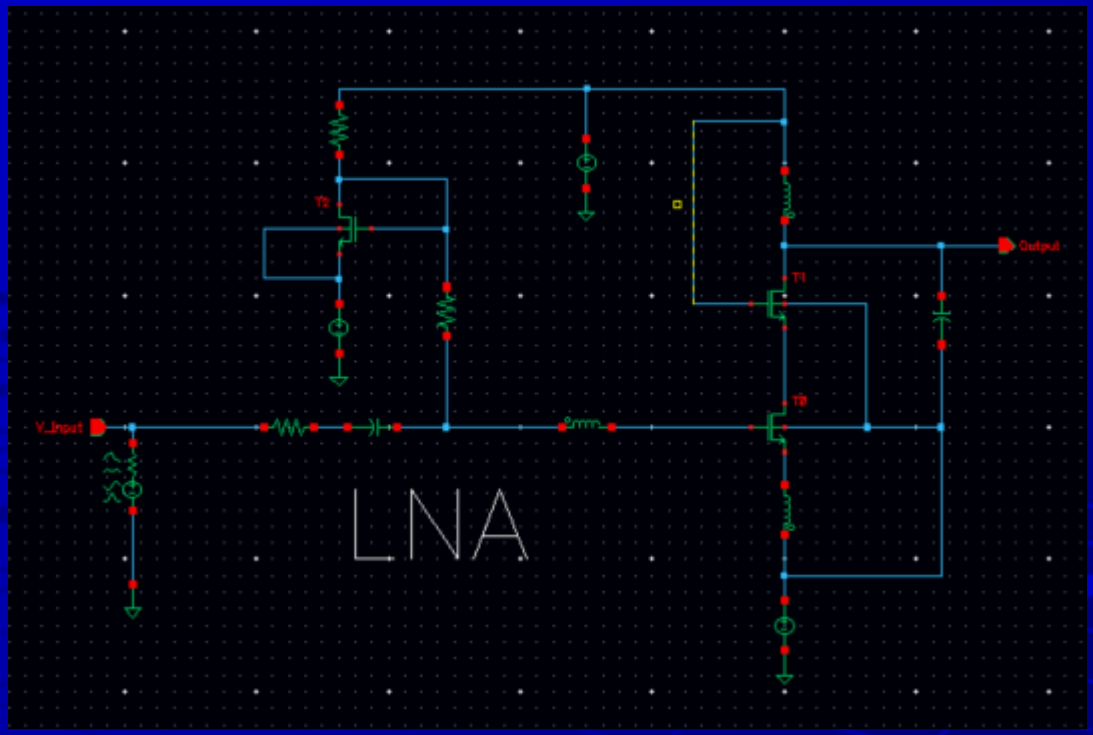
S_{11} = -23 dB (much better than -11 dB)
S_{21} = 23 dB

Input P1dB = -15.4 dBm

Third Order Intercept point TOI, IIP_3 = -6 dBm

Plots from the actual simulations are on the next several slides.

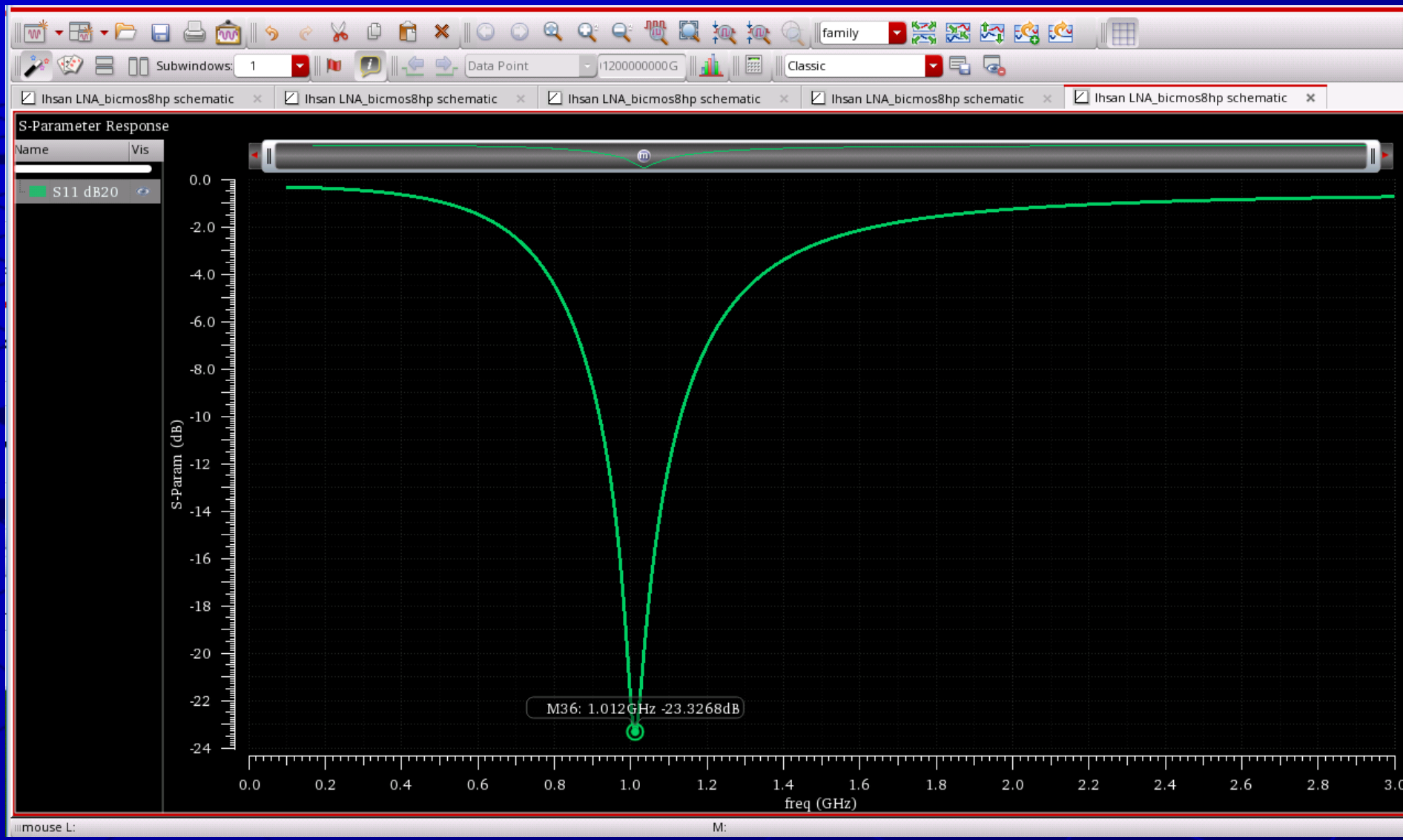
LNA



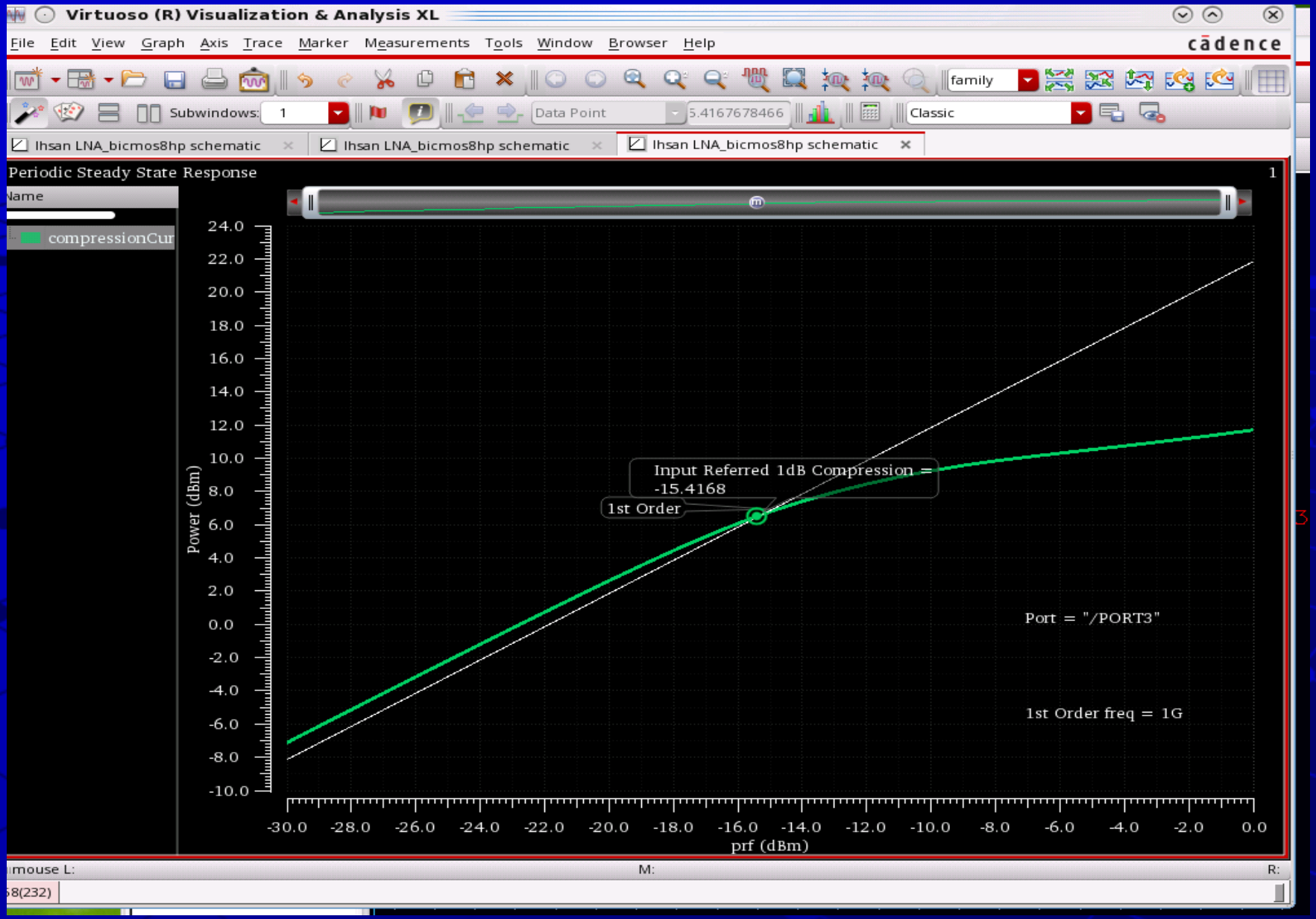
LNA Design Consideration

- Noise performance
- Power transfer; Amplifies input to output
- GAIN of LNA: $\frac{V_{out}}{V_{in}} = \frac{-g_m R_P}{1+g_m \omega L_S}$
- Impedance matching to Antenna (50Ω)
- Matching $\frac{g_m L_S}{C_{gs}}$ = 50Ω (real part and noiseless)
- Bandwidth. Wideband LNA can be designed
- Stability. LNA is stable. [Tool used by Cadence]
- Linearity [1dB compression point]

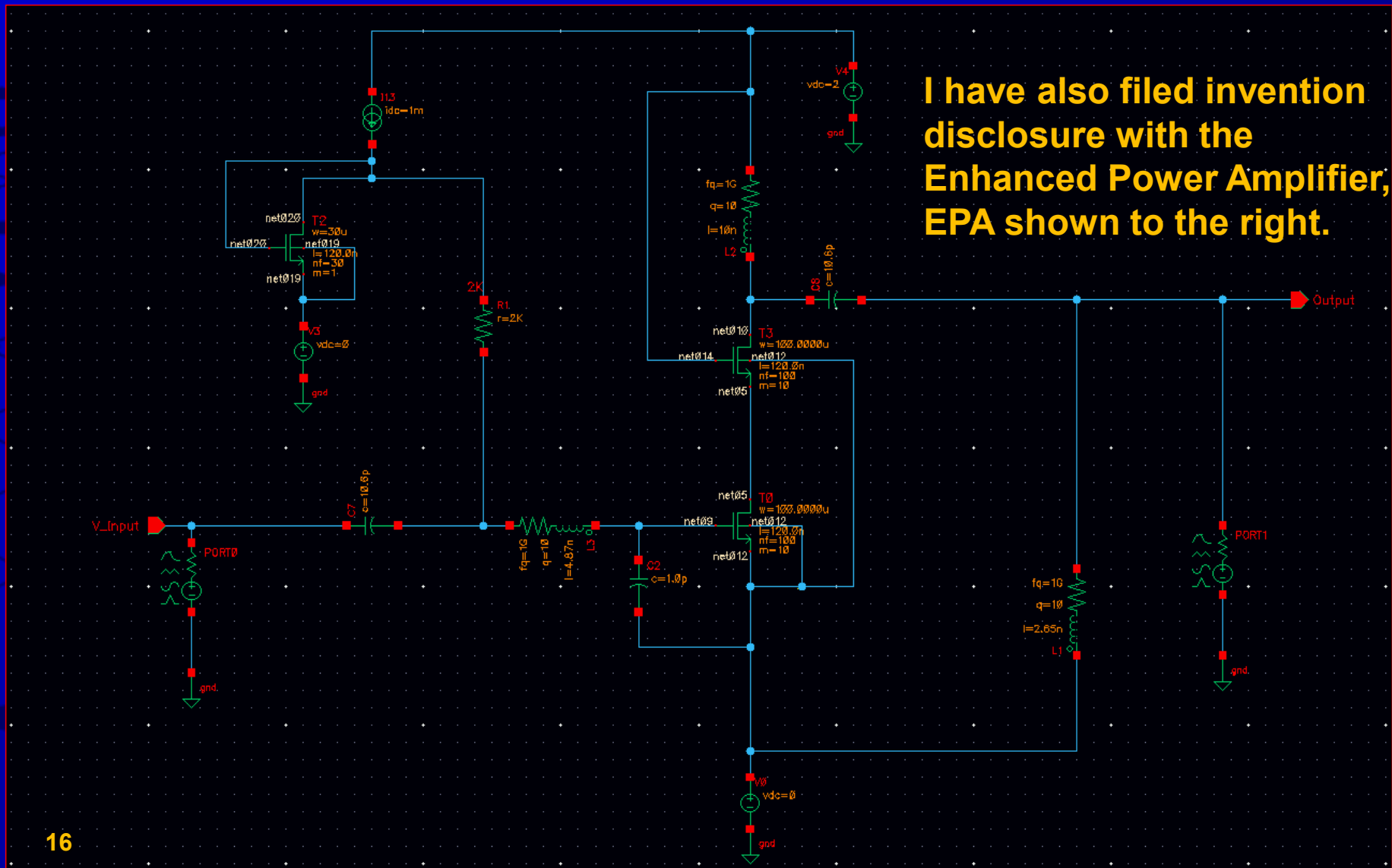
S_{11} of the LNA in dB



Cont'd. LNA P1dB Simulations



Cascaded PA: Better Stability, Higher Linearity & Lowering the miller effects



I have also filed invention disclosure with the Enhanced Power Amplifier, EPA shown to the right.

Power Amplifier (PA)

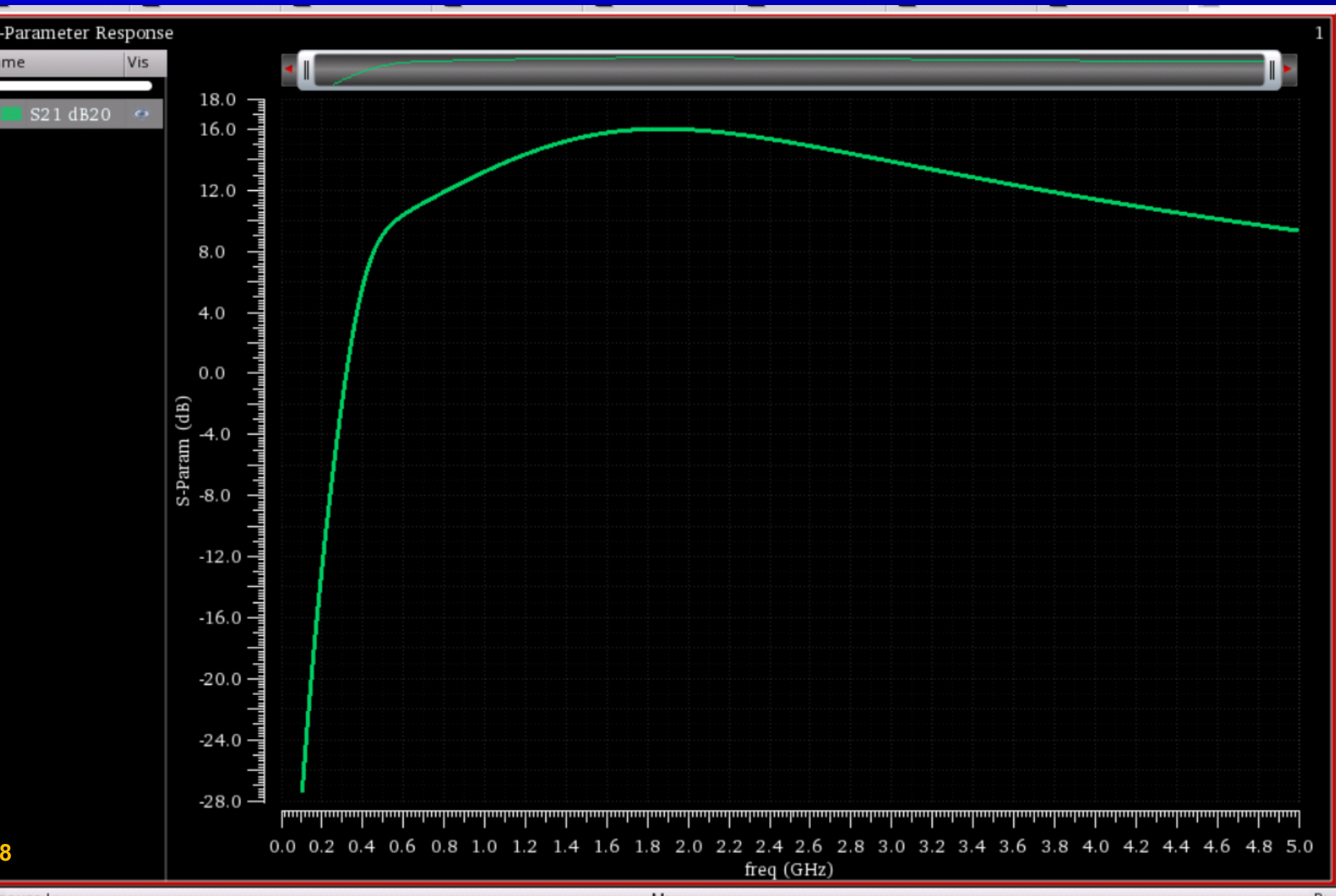
- Supply is limited (for example 1.8 V)
- Device Breakdown Voltage is limited

$$V_{GS}\ V_{GD}\ V_{DS} < 1.8\text{ V} + 10\% = 2\text{ V}$$

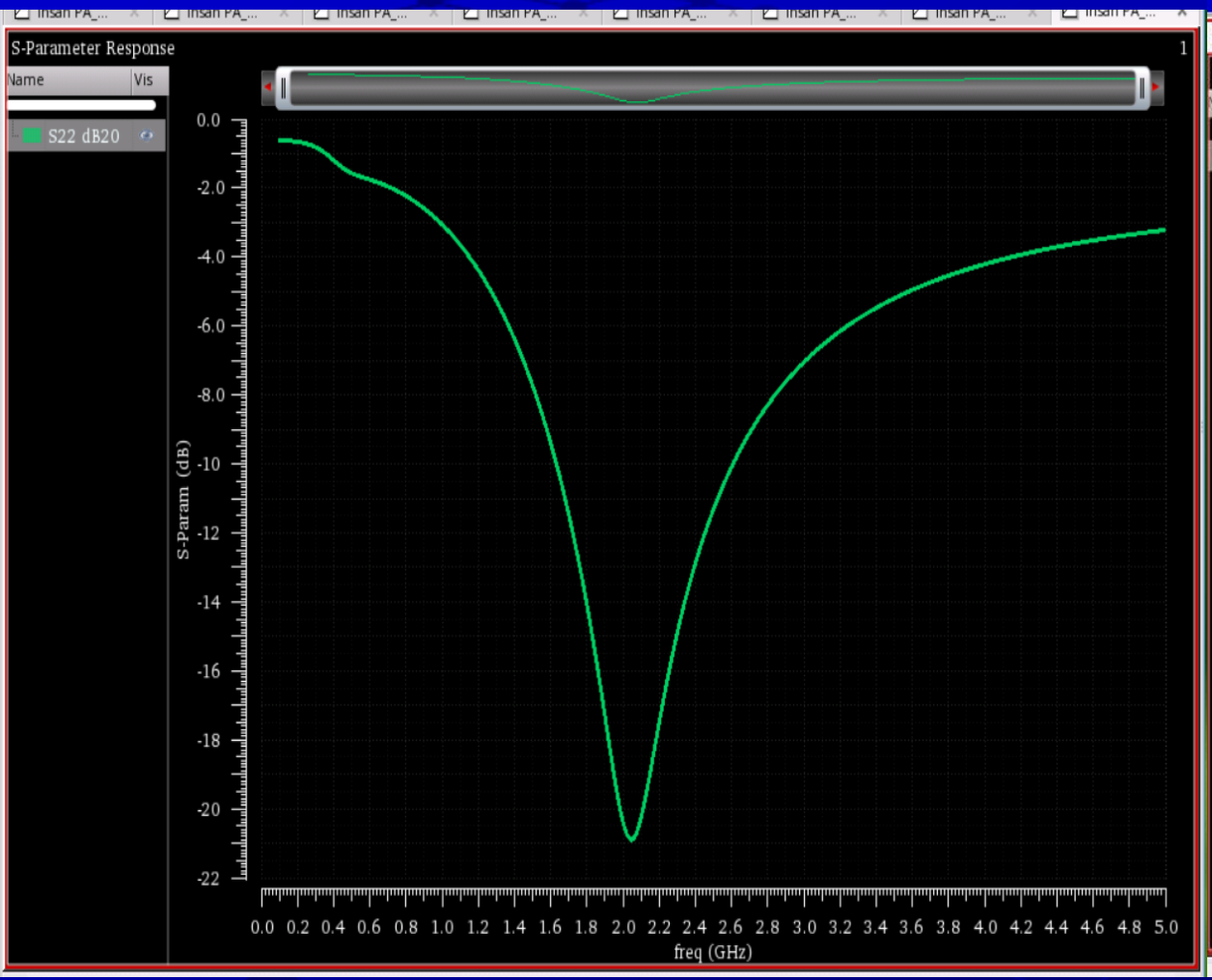
This is DC, less than 2 V but AC can be > 2.0V

- Impedance matching to output (50Ω)
- Create highest swing, that is still safe at the PA output. This is to maximize the power at the output (e.g. if P_{out} = 100mW and P_{in} = 1mW, then).
- $PA_{GAIN} = 10\ log_{10} \frac{P_{out}}{P_{in}} = 20$ dB

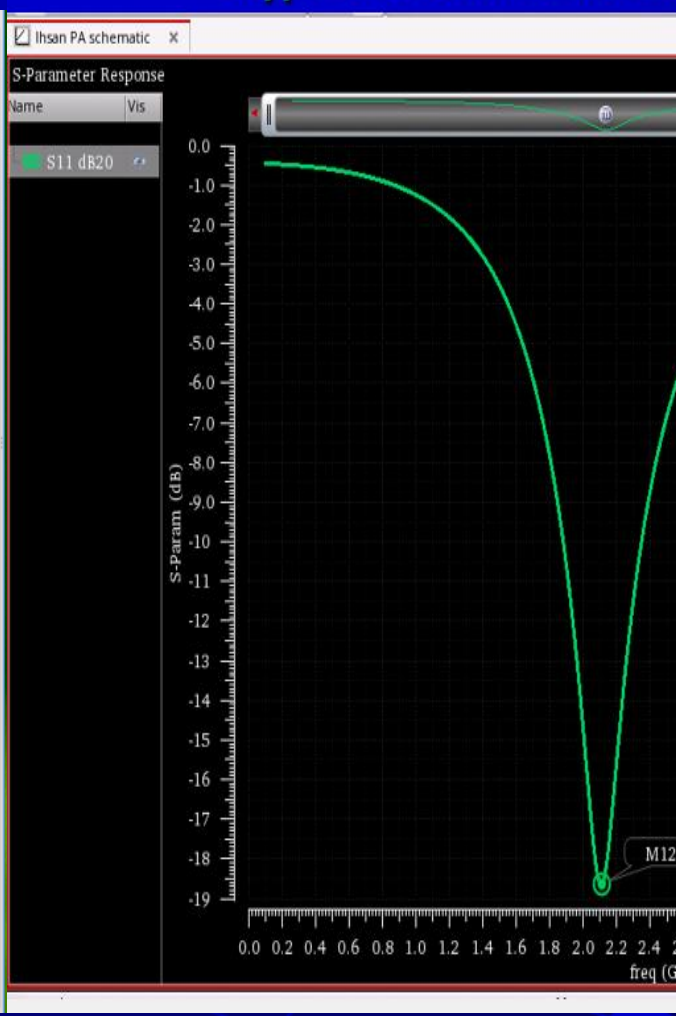
GAIN: S_{21} of the PA = 16dB



S_{22} : The PA can run at 2 GHz



S_{11} of the PA in dB



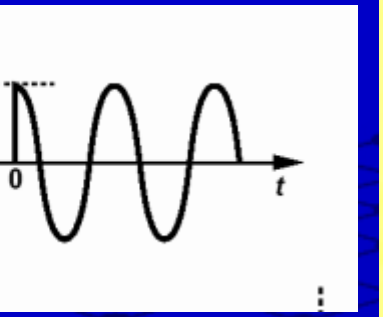
RF_analog Design: Voltage Controlled Oscillator, VCO.

SUMMARY:

Center frequency: Around: 2.45GHz. Tuning range: +/- 200MHz about center frequency. This may work with process and temperature variations.

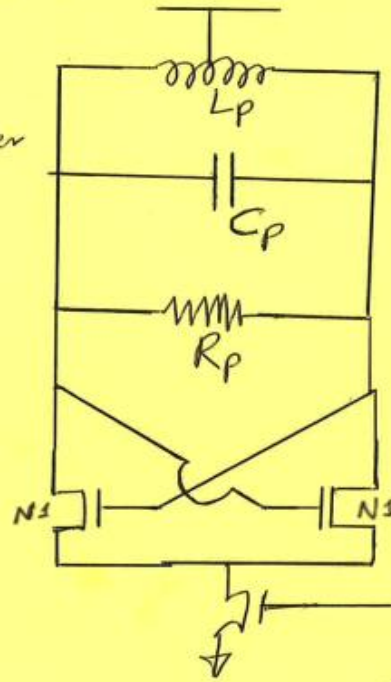
Output power: At least +6dBm across the tuning range, measured into a 100Ω differential load.

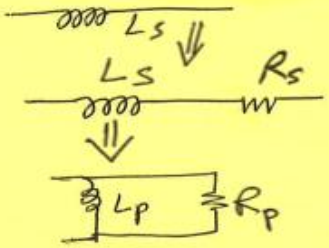
Comes along with a flavor of low phase noise.
Mitigated Phase (PN) and Flicker Noise.
Techniques with Cap Banks, Varactor.



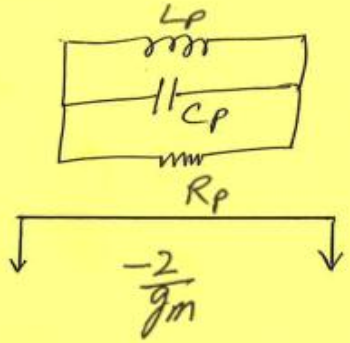
LC VCO

R_p from L_s, LC tank losser





Will Oscillate when the Real part of equivalent Impedance is Negative.



To oscillate,

$R_p > \left|\frac{2}{g_m}\right|$

Not too big, Power ↑, %

CMOS twice the Voltage than NMOS.

Power also ↑ TWICE.

6dB better.

VCO Design project.

VCO oscillate of the LC Tank:

To start oscillate, you need to have

$$2 / g_m < R_p$$

VCO is basically a gain stage and a LC tank.

IBM CPU Design from 130nm CMOS to 45nm SOI Technology.

Challenges of Design in SOI Technology from CMOS.

- When a technology gets shrunk two things increase:
- 1. Variations and
- 2. Leakage Current.

- Furthermore, it is almost impossible to achieve radiation hardness on modern process nodes.

Redesigned IBM Microprocessor from 130nm CMOS to 45nm SOI Technology.

- I have experience in Silicon Debugging. Simulated and checked a lot of functionalities and sanity of the electronic design.
- Learned from the failure analysis. This experience in hardware debugging however, is considered a precious experience in the industry…it goes in your favor.
- I've designed multiple blocks in the IBM Microprocessor shown here:
- This project was a very successful project.

Broadway

IBM Broadway microprocessor from the inside of a Wii. The reference to Canada in the pictu is related to where it was packaged i.e. by IB Canada in Bromont.

General information

Summary of Low Power Design.

Knobs for Low Power Design	CHANGE	Threshold V_{th}	Leakage Current, I_{Leak}
Device Length l	IF DECREASES	DECREASES	INCREASES
Device Width W	IF DECREASES	INCREASES	DECREASES
V_{BULK}	IF DECREASES	INCREASES	DECREASES
Doping-Cont N_A	IF INCREASES	INCREASES	DECREASES
Gate Thickn T_{Si}	IF DECREASES	DECREASES	INCREASES
Temperature	IF INCREASES	DECREASES	INCREASES

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Leadership Skills and Experience

- A) As a Lead engineer, trained and guided Electronic Engineers in the high tech at IBM, LM and NG.
- B) Coordinated and led RF Engineers for the RF Lab and wrote Test Procedures for the RF Team.
- C) Experience with leading a team of engineers.

Software experience on projects.

MATLAB:

- Simulated different complex equations and their graphs. GPS III Satellite project.
- Goal was to determine the Gravity of the Moon.

- Extensively worked in Unix (also in Linux) env.

- Written Assembly and Scripting Languages.

- Courses taken in College: C++/C#, Python and Java.

Thank you.